Firmware Flexibility using Intel® Firmware Support Package

Vincent Zimmer – Senior Principal Engineer, Intel Corporation
Agenda

• Overview of the Intel® Firmware Support Package (Intel® FSP) to encapsulate Intel® silicon initialization

• Scaling platform initialization with the Intel FSP and open source Intel® Architecture (IA) firmware ecosystems

• Details on building an open source IA platform with Intel FSP

• Full openness

• Summary and next steps
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The Intel® Firmware Support Package (Intel® FSP)

Intel® Firmware Support Package (Intel® FSP) components

• CPU, memory controller, and chipset initialization functions as a binary package
• Provides silicon initialization ingredients
• Plugs into existing firmware frameworks
• Integration guide, includes API documentation

Intel FSP is currently available for the many Intel® hardware-producing divisions
From IDF 2013 Applying Intel® Firmware Support Package to Open Source EDK II

EDK II provides the framework ("Green H")

Intel® Firmware Support Package (Intel® FSP) provides low level of silicon initialization
Applying “Produced” Intel® Firmware Support Package (FSP) to “Consuming” IA firmware

UEFI/PI Scope - Green “H” w/ EDK2

- OS
  - UEFI Specification
  - Platform Drivers
  - Intel® FSP
  - Hardware/Silicon

FSP

- Glue Code (PEI Core / Arch PPIs)
- Single Si Init Binary
  - CPU
  - SA
  - PCH
  - ME

Payload
- coreboot ramstage
- Intel® FSP
- coreboot romstage
- Hardware/Silicon

PEI/DXE PI Foundation
Modular Components (from IDF 2013)
**Intel® FSP Producer**

- Examples of binary instances on [http://www.intel.com/fsp](http://www.intel.com/fsp) with integration guides
- This includes hardware initialization code that is EFI Developer Kit II (EDK II)-based PEI Modules (PEIM’s)
- Modules are encapsulated as a UEFI PI firmware volume w/ extra header
- Configure w/Vital Product Data (VPD)-style Platform Configuration Data (PCD) externalized from the modules
- Resultant output state reported via UEFI Platform Initialization (PI) Hand Off Block (HOB)
- Present 1.0 specification at [FSP 1.0 External Architecture Specification (EAS)](http://www.intel.com/fsp)
The Source for the Intel® FSP Producer Code

• CPU and chipset-specific code for PEIM’s inside of the Intel FSP can be open or closed, added to...

• PEI core and infrastructure code at https://svn.code.sf.net/p/edk2/code/trunk/edk2/MdePkg and https://svn.code.sf.net/p/edk2/code/trunk/edk2/MdeModulePkg

• And the code to create the Intel FSP interfaces can be found at https://svn.code.sf.net/p/edk2/code/trunk/edk2/IntelFspPkg/

Intel FSP can encapsulate IP protected initialization code PRODUCED by Intel business units
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Intel® FSP Consumer

• Consumer Firmware can be bootloaders from board support packages, traditional BIOS, UEFI/PI based EDK II firmware, or other embedded software solutions

• Firmware to absorb, integrate, or ‘consume’ the Intel FSP binary

• Consistent consumer code in the open source Intel® Architecture firmware up streams

• Enables fully open work-flow of using Intel FSP and open source IA firmware code
Intel® FSP Boot Flow

Reset Vector
- Switch to 32-bit Mode
- Find FSP Entry Point
- Jump to FSPinit

Intel® Firmware Support Package (Intel® FSP)
- Load Microcode
- Temp Ram Init
- Mem Init
- Companion Chip Init
- Processor Init
- NotifyPhase Code

Parse Return Data
Platform Init
Bus and Device Init
NotifyPhase
Boot Device Init
Load OS or other payload
NotifyPhase
PostPciEnum
ReadyToBoot

Boot Loader or "FSP Consumer"
- Intel FSP from "FSP Producer"
**Intel® FSP External Interfaces**

APIs published by the Intel FSP Producer and invoked by the Consumer

- **TempRamInit** - Enables cache for using as temporary memory and code caching
- **FspInit** - Performs the processor and companion chipset initialization
- **NotifyPhase** - Hooks for certain phase during the platform initialization

Intel FSP Producer/binary creates the UEFI PI Hand-off Blocks (Vol 3 of the UEFI PI spec)

- Contains basic platform information

![Diagram showing Intel FSP External Interfaces](attachment:image.png)
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### 2 Consumers: EDK II firmware and coreboot*

<table>
<thead>
<tr>
<th>Functionality</th>
<th>coreboot</th>
<th>UEFI / PI</th>
</tr>
</thead>
<tbody>
<tr>
<td>The reset vector and pre cache-as-ram setup</td>
<td>bootblock</td>
<td>Security Phase (SEC)</td>
</tr>
<tr>
<td>Cache as Ram setup, early silicon initialization, memory setup. Covered largely by Intel® Firmware Support Package</td>
<td>romstage</td>
<td>Pre-EFI Initialization (PEI) Create HOBs</td>
</tr>
<tr>
<td>Normal device setup and mainboard configuration. Publish SMBIOS/ACPI Tables</td>
<td>ramstage</td>
<td>Early Driver Execution Environment (DXE)</td>
</tr>
<tr>
<td>Memory map hand-off</td>
<td>CBMEM</td>
<td>UEFI Memory Map</td>
</tr>
<tr>
<td>The OS or application bootloader</td>
<td>payload</td>
<td>DXE BDS and UEFI Drivers</td>
</tr>
</tbody>
</table>

*Note: The table above outlines the different stages of the boot process, indicating which functionalities are handled by coreboot or UEFI/PI.
EDK II based Intel® FSP Consumer Details

Following discussion

IntelFspPkg
PlatformFspPkg
SiliconPkg
EDKII Pkg
FSP.bin

coreboot*
fsp lib
EDKII Pkg
PlatformPkg
IntelFsp
WrapperPkg

Intel® Firmware Support Package (Intel® FSP)
EDK II based Intel® FSP Consumer Flow

- Generic EDK II code, the FSP Wrapper
- [https://svn.code.sf.net/p/edk2/code/trunk/edk2/IntelFspWrapperPkg/](https://svn.code.sf.net/p/edk2/code/trunk/edk2/IntelFspWrapperPkg/)
- Allows for integration of Intel® Firmware Support Package binary into EDK II-based platform code
- Some sample platform code at [http://uefiddk.com](http://uefiddk.com)
coreboot* based Intel® FSP Consumer Details

Following discussion

coreboot*

fsp driver

EDKII Pkg

IntelRcPkg

PlatformFspPkg

FspPkg

FSP.bin

EDKII Pkg

PlatformPkg

FspWrapperPkg
<table>
<thead>
<tr>
<th>coreboot* driver</th>
<th>Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>find_fsp</td>
<td>Function to find the FSP in memory</td>
</tr>
<tr>
<td>fsp_early_init</td>
<td>FSP memory and early device setup function. Called in romstage by the chipset driver</td>
</tr>
<tr>
<td>romstage_fsp_rt_buffer_callback</td>
<td>Callback from fsp_early_init for mainboard specific RT buffer customizations (soldered down memory timings, etc.)</td>
</tr>
<tr>
<td>FspNotify</td>
<td>There are two notify calls in ramstage. AfterPciEnumeration during device finalize and ReadyToBoot during chip finalize.</td>
</tr>
<tr>
<td>save_mrc_data</td>
<td>Called in romstage after fsp_early_init to save the memory configuration to CBMEM</td>
</tr>
<tr>
<td>update_mrc_cache</td>
<td>Moves the mrc data from CBMEM to NVRAM in late ramstage</td>
</tr>
</tbody>
</table>
The EDK II and coreboot* open source ecosystems can CONSUME FSP’s with the upstreamed FSP wrapper package & driver
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Many Paths for Enabling

- We’re moving into a world where it is easier to work with Intel® platforms
- Open platforms, open source
- Intel® Unified Binary Management System (Intel® UBMS)
- Development kits, Reference boards
- There is also a full open source EDK II option
  - See full platform sources for Intel® Quark™ SoC, including a feature rich UEFI build
Intel® Quark™ SoC – Hardware Overview

- 32 bit Intel® Pentium® ISA-class processor
- PCI
- USB
- I2C
- Single core
UEFI for Intel® Quark™ SoC

• First fully open source Intel-based platform

• Builds on Intel® UDK2010 packages like MdePkg, MdeModulePkg w/ a 32-bit build, adding
  - IA32FamilyCpuBasePkg
  - QuarkPlatformPkg
  - QuarkSocPkg

• Standard build is 1 Mbyte image w/full features
  - Capsule update, SMM, S3, PCI, recovery, full UEFI OS support, FAT OS support, UEFI variables
UEFI for Intel® Quark™ SoC

- A modular firmware architecture like UEFI PI and code-base like EDK II allows for scaling the technology
- Fixed function UEFI OS load experiences can scale in size
- Introducing “TinyQuark” open source example
  - 64 kbyte to boot
  - UEFI-aware
  - Yocto* image from SPI NOR flash

<table>
<thead>
<tr>
<th>Module</th>
<th>Size (K)</th>
<th>%</th>
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</thead>
<tbody>
<tr>
<td>Generic</td>
<td>34</td>
<td>50%</td>
</tr>
<tr>
<td>Silicon</td>
<td>10</td>
<td>14%</td>
</tr>
<tr>
<td>Platform</td>
<td>24</td>
<td>36%</td>
</tr>
</tbody>
</table>

Many paths for enabling, including full openness
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Summary

• Intel® Firmware Support Package (Intel® FSP) can encapsulate IP protected initialization code PRODUCED by Intel business units

• The EDK II and coreboot* open source Intel® Architecture (IA) firmware ecosystems can CONSUME FSP’s with the upstreamed FSP wrapper package and driver code

• Beyond mixing binary FSP and source, a full open source EDK II experience is possible, as noted by the Intel Quark Firmware
Next Steps

• Start to examine the Intel® Firmware Support Package (Intel® FSP) collection at intel.com/fsp, support code at tianocore.org, and sample projects at uefidk.com

• Provide Intel feedback as Intel FSP 1.0 EAS evolves going forward for new platform topologies FSP 1.0 External Architecture Specification (EAS) and whitepaper at FSP on EDKII Whitepaper

• Build more platforms with open source platform packages on www.tianocore.org and www.coreboot.org

• Evaluate the first fully-featured platforms on uefidk.com, like Intel® Quark™ SoC https://communities.intel.com/docs/DOC-22226 and Tiny Quark https://uefidk.com/content/get-started-intel-galileo-development-board and whitepaper at TinyQuark Whitepaper
Additional Sources of Information

- A PDF of this presentation is available from our Technical Session Catalog: www.intel.com/idfsessionsSF. This URL is also printed on the top of Session Agenda Pages in the Pocket Guide.

- More web based info:
  www.tianocore.org
  www.intel.com/fsp
  www.uefidk.com
  www.coreboot.org

- More on topics discussed in this presentation:
  see upcoming book
  *Embedded Firmware Solutions*
  http://www.apress.com/9781484200711
Participate for Chance to Win!!

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• Get your RFID/USB wristband and details at the Software & Services Pavilion in the Technology Showcase, or at our mobile carts outside Moscone West.

• Once you register, you’re connected to:
  - Software and services content
  - Tracking earned coins for the “Surf the Code” game and other prizes
  - Your own 3D avatar with 10 coins... Play the game, share with friends

• Visit the Software & Services Pavilion to earn more coins
  - Talk with Intel experts about your development needs and plans
  - Tinker on your own time with self-run labs, source code, tools
  - Swipe your wristband on the Galileo Scan Stations to get coins

• Play to Win in the Software & Services Pavilion
  - Get 5 coins to play “Surf the Code”... Gift cards for three highest scores!
  - Get 10 coins to get your 3D avatar... And enter daily drawing for tablets and 2-in-1s
  - Get 15 coins for your King Code t-shirt, and increase total game score potential

Don’t let the fun stop!
Daily lunch at food trucks
### Other Technical Sessions
from Software Services Group & System Tools and Technology Tracks

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<th>Title</th>
<th>Day</th>
<th>Time</th>
<th>Room</th>
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<tbody>
<tr>
<td>SFTS005</td>
<td>Oracle* Exalytics in the Speed of Thought: Extreme Scaling on Intel Xeon Processor E7</td>
<td>Tues</td>
<td>4:00</td>
<td>2007</td>
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<tr>
<td>SFTS006</td>
<td>Creating Immersive Augmented Reality Experiences on Android* Mobile Platforms Based on Intel® Architecture</td>
<td>Tues</td>
<td>5:15</td>
<td>2007</td>
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<tr>
<td>STTS001</td>
<td>Firmware Flexibility Using the Intel® Firmware Support Package</td>
<td>Thurs</td>
<td>9:30</td>
<td>2008</td>
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<td>STTS002</td>
<td>Simplifying Firmware Development with Intel® Unified Binary Management Suite</td>
<td>Thurs</td>
<td>10:45</td>
<td>2008</td>
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<tr>
<td>STTS003</td>
<td>Complex Systems Become Simple: Internet of Things with Wind River Simics*</td>
<td>Thurs</td>
<td>1:00</td>
<td>2008</td>
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<tr>
<td>BIGS004</td>
<td>Accelerating Hadoop* Performance on Intel® Architecture Based Platforms</td>
<td>Thurs</td>
<td>1:00</td>
<td>2004</td>
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<td>IOTS007</td>
<td>Intel® Firmware Support Package for Internet of Things</td>
<td>Thurs</td>
<td>2:15</td>
<td>2001</td>
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<tr>
<td>STTS004</td>
<td>Software Based System Power and Thermal Optimization Technology</td>
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</table>

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